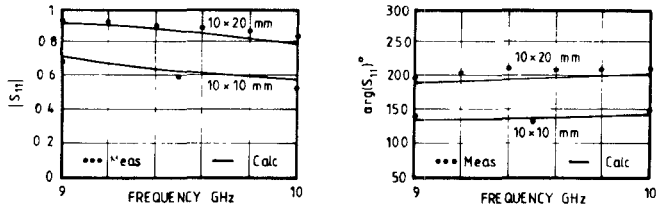

Fig. 3. Measured (dotted lines) and calculated values (solid lines) for the reflection coefficient and phase of the equivalent circuit

A is therefore the necessary normalization constant of $e(x, y)$. The expression for V^2 follows from (12):

$$V^2 = -k_z^2 + \frac{(\epsilon_r - 1)k_0^2}{A} \cdot (k_z\beta)^2/\epsilon_r \left[l + \frac{\sin 2\pi l/a}{2\pi/a} \right] \cdot \left[\frac{1}{2}b - \frac{\sin \beta b}{2\beta} \right] - \left[\frac{k^2 - \beta^2}{\epsilon_r} \right]^2 \cdot \left[l + \frac{\sin 2\pi l/a}{2\pi/a} \right] \cdot \left[\frac{1}{2}b + \frac{\sin \beta b}{2\beta} \right] - \left[\frac{\pi}{a} \cdot \frac{\beta}{\epsilon_r} \right]^2 \cdot \left[l - \frac{\sin 2\pi l/a}{2\pi/a} \right] \cdot \left[\frac{1}{2}b - \frac{\sin \beta b}{2\beta} \right] \Bigg\}. \quad (14)$$

After substitution of A into (14), a parameter K is defined as

$$K^2 = -k_z^2 + V^2.$$

The differential equation (10) now is

$$d^2f(z)/dz^2 - K^2 f(z) = 0 \quad (15)$$

and the solution to this is

$$f(z) = f_e + f_o \quad (16)$$

where f_e and f_o are the even and odd parts of $f(z)$, and

$$f_e = D_e \cosh Kz \qquad f_o = D_o \sinh Kz. \quad (17)$$

If (3), (4), and (17), together with their derivatives, are equated at the discontinuity boundary, which is a static approximation, then the even and odd mode phase shifts are given by

$$\cot \eta_e = \frac{-\sin k_z d + k_z/K \coth Kd \cos k_z d}{-k_z/K \sin k_z d \coth Kd - \cos k_z d} \quad (18)$$

$$\cot \eta_o = \frac{\cos k_z d + \sin k_z d\, k_z/K \tanh kd}{k_z/K \cos k_z d \tanh Kd - \sin k_z d} \quad (19)$$

where the wavenumber in the z direction is k_z. The transverse wavenumbers, α and β, are solutions of the transcendental equation

$$\beta \tan \frac{1}{2}\beta b = \epsilon_r \alpha \quad (20)$$

subject to the constraint

$$\alpha^2 + \beta^2 = k_0^2(\epsilon_r - 1) \quad (21)$$

while the guide wavenumber is calculated from

$$k_z = \sqrt{k^2 - (\pi/a)^2 - \beta^2}. \quad (22)$$

It is now possible to calculate the equivalent admittance network for holes of any given dimension using (6) and (7).

III. Experimental Results

The reflection coefficient and phase angle of the equivalent T section of two rectangular holes, of dimensions 10×20 mm and 10×10 mm, respectively, were measured, and the data are plotted in Fig. 3(a) and (b) together with the theoretically calculated values using the equations developed above. The agreement between the various sets of values is good.

IV. Conclusions

A theoretical analysis that makes it possible to calculate the equivalent circuit for a rectangular discontinuity in NRD waveguide has been presented and verified experimentally. A major advantage of the theory is that the equations are in closed form.

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Frequency Normalization of Constant Power Contours for MESFET's

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***Abstract*—The constant power contours have been measured on MESFET's with different doping profiles over the frequency range 8–16 GHz for a fixed input power level at different bias points. At each frequency, the contours are normalized with respect to the load for maximum power output; within experimental accuracy, the normalization holds fairly well independent of frequency under certain limits.**

I. Introduction

The design of a power amplifier over a wide frequency range involves, in general, the measurement of constant power contours and constant efficiency contours at different frequencies at some given bias point. The measurement of these contours at different frequencies is very time-consuming. Moreover, one may not have the experimental setup to find the contours at the frequencies of interest. The present investigation shows how these curves can be predicted at other frequencies under certain limits. The concept is an extension of small-signal mismatch circles. In case of large-signal applications, the mismatch contours are no longer circles, because of the way the saturation current and breakdown voltage limits are attained. The contours present some reflection coefficient loci with respect to a given load. The idea was first proposed by Cripps [1]; it has been extended in this paper over a wide frequency range.

In the present case, the contours are normalized with respect to the conjugate of load that gives maximum power with a given input power. The conjugate of optimum load impedance to yield maximum power output may be represented at any given frequency by a parallel combination of R and C. The values of R

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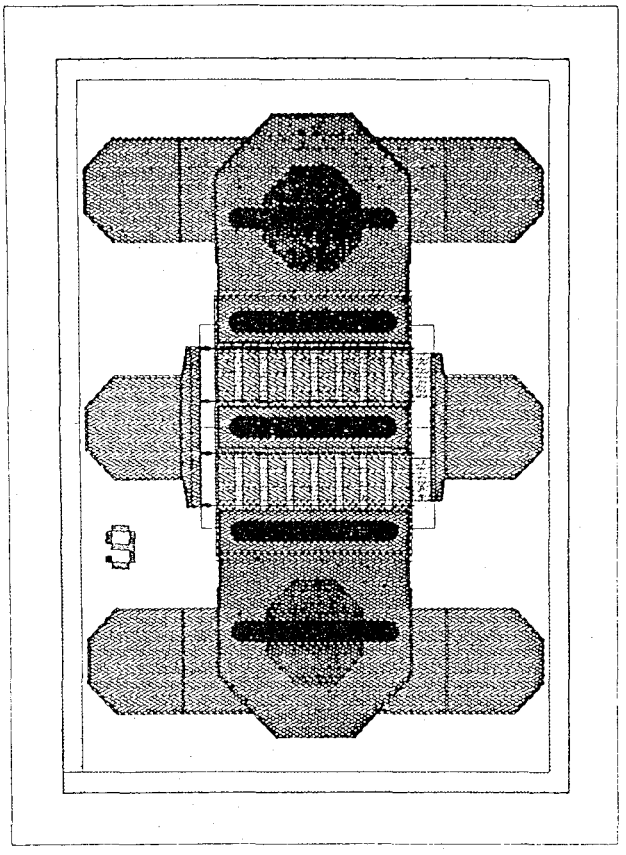


Fig. 1. Horizontal layout of the FET under study.

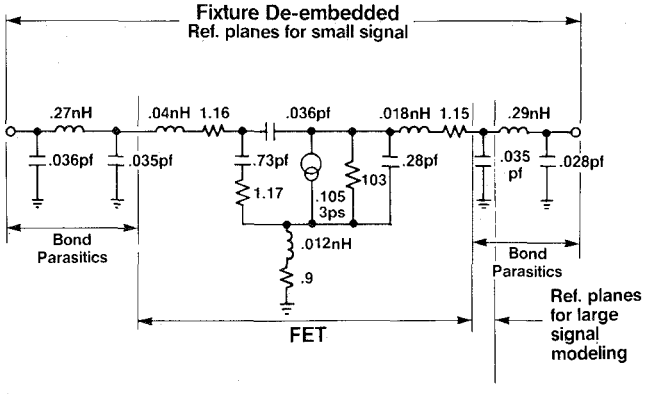


Fig. 2. Small-signal model of impulse doped FET at one bias point: $V_D = 6.5$ V, $I_{DS} \simeq \frac{1}{2} I_{DSS}$. It corresponds to the bias point in Fig. 4(b). All the bias-independent parasitics are estimated by fitting the measured S parameters over four bias points simultaneously.

and C remain very much unchanged over the frequency range of interest only if the device I–V and breakdown characteristics remain almost unchanged (these two characteristics affect R) and if the parasitic and/or distributed effects can be neglected (these will affect the effective value of C). The devices (gate length $\simeq 0.5$ μm) we have chosen for investigation have a total gate width of 800 μm (four fingers, 200 μm each). Fig. 1 shows the layout of such a device. Fig. 2 shows the equivalent circuit of a device with a given doping profile at a given bias point. Since the lumped element equivalent circuit model was obtained by fitting the measured S parameters simultaneously at four bias points for a given device over the frequency range 2–18 GHz and

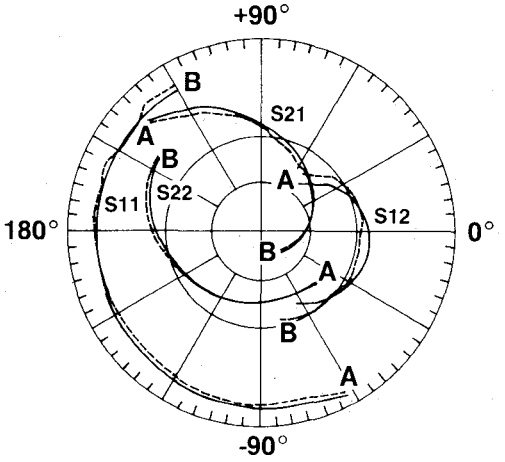


Fig. 3. A sample fitting of the de-embedded measured S parameters on polar chart. —— model; ---- measured. A: 2 GHz, B: 18 GHz. Radius is "1" for $S11$ and $S22$, "7" for $S21$, and "0.1" for $S12$.

the fitting was very good (Fig. 3), we assume the distributed effect is negligible for the devices at least up to 18 GHz. It is imperative to make a close estimate of the bonding wire inductance; otherwise the effective value of C will change with frequency due to bonding wire inductance. Care is taken to model the FET properly with the associated parasitics after following a fixture de-embedding procedure similar to TSD [2]. The parasitics due to air bridges over the drain fingers will increase the source-to-drain capacitance, and the change in the source inductance (which is quite low) due to air bridges in our case is negligible.

So the value of C remains almost unchanged. This has been verified by taking measurements at different frequencies and also at different bias points. In the present case, the value of R was constant within experimental accuracy. So the device I–V and breakdown characteristics have not changed appreciably over the measurement frequency range. It should be mentioned at this point that the maximum power at each frequency is not the same. The contours are relative to maximum power only. The measurement of maximum power was taken approximately at the 2–3 dB compression point, and it is assumed that there will be enough nonlinearity to compress the contours inside the small-signal mismatch circles, whose radii on Smith charts can be shown to be

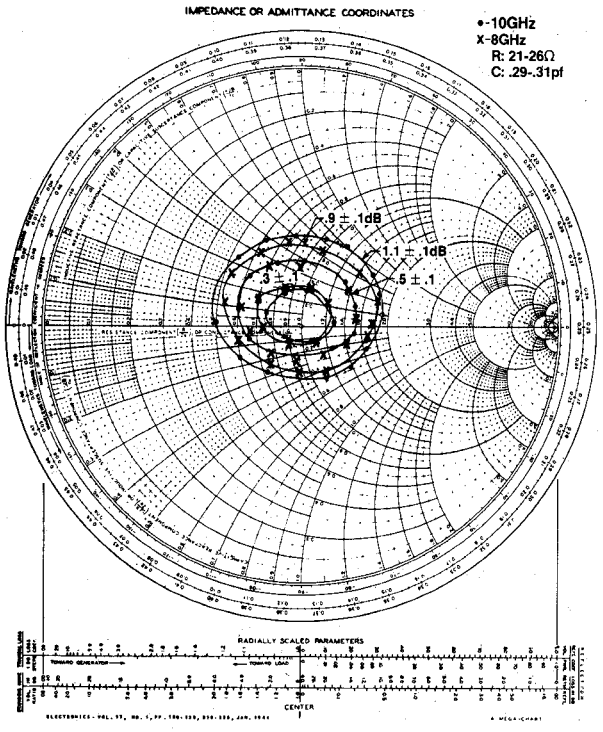
$$|\rho|^2 = 1 - 10^{-\eta/10} \tag{1}$$

where ρ is the reflection coefficient of the load with respect to Z^*_{opt} (Z_{opt} being the load for maximum power), and η is the amount of mismatch in dB. All the constant power contours must lie within (1).

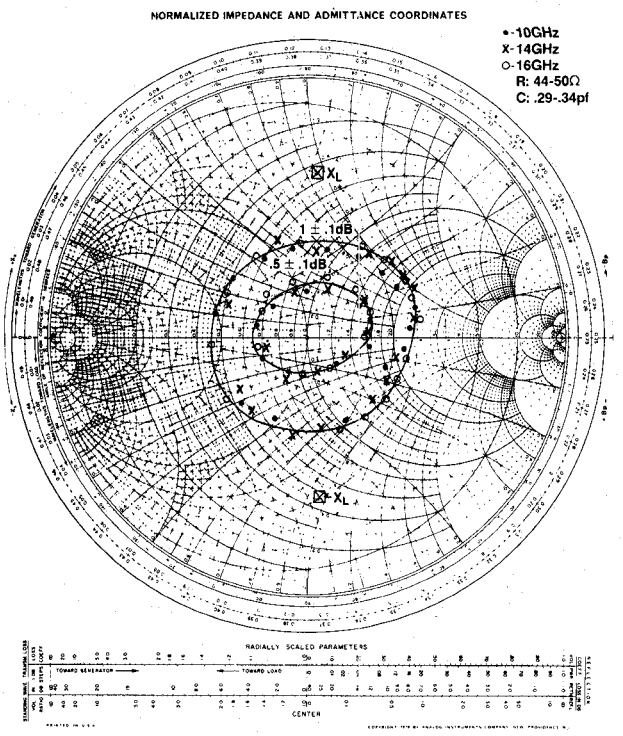
We should point out that the proper values of R and C are necessary to denormalize the normalized contours. As such, the values of R and C can be changed by shifting the reference plane without affecting the normalization procedure.

II. Measurement

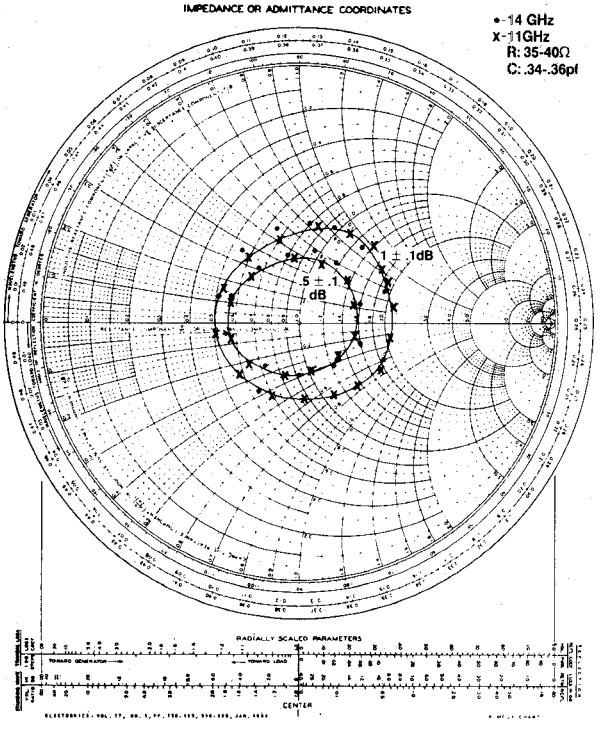
We will report results on two devices with different doping profiles. Device A is uniformly doped (2E17) with no capping layer. Device B is impulse-doped (a highly doped channel layer, a lower doped layer to which the gate is recessed, and a very highly doped cap layer for good ohmic contacts and protection from drain burnout). A similar type of device (as device B) has been reported recently in [3]. All wafers were grown by molecular



(a)



(b)



(c)

Fig. 4. Power contours for different devices over 8–16 GHz range. The center of the Smith chart corresponds to Z^*_{opt} for maximum power output. The equivalent $R\|C$ for Z^*_{opt} values are shown at the right-hand top corner of each figure. (a) Impulse doped (W #155, R #8, D #15, DEV B): $V_D = 4.9$ V, $I_{DS} \simeq 15$ percent I_{DSS} ($I_{DSS} \simeq 390$ mA/mm). (b) Impulse doped (W #155, R #8, D #15, DEV B): $V_D = 6.5$ V, $I_{DS} \simeq 50$ percent I_{DSS}. (c) Flat doped (W #148, R #24, D #15C, DEV A): $V_D = 5.0$ V, $I_{DS} \simeq 25$ percent I_{DSS} ($I_{DSS} \simeq 430$ mA/mm).

beam epitaxy, with a 1 μm undoped expitaxial buffer layer to provide device isolation. The measurement is made with a constant input power level of 16–17 dBm at each frequency. An automatic load-pull setup has been used to draw the constant power contours. Due to tuner resolution, it is sometimes more convenient to draw contours that are slightly off the target values. Each contour is drawn within the maximum deviation limits of ± 0.1 dB.

Figure 4 shows the normalized power contour of these devices. We also show the range of R and C values that have been obtained through optimum load measurement. The value of R changes with the bias condition; it remains almost constant with frequency and shows that the device I–V and breakdown characteristics have not changed appreciably over the frequency range of interest. C is very constant over the frequency range. It shows that both the distributed and the parasitic effects are not prominent for the device under investigation.

In Fig. 4, we show the normalized power contours (the center of the Smith chart being Z^*_{opt}) for which the input reflection coefficient is maintained less than -12 to -13 dB. The power contours, which are highly mismatched with respect to the load impedance for maximum power (in our case, more than 1 dB at 17 dBm input power), tend to increase the average gate current. As a result, both the input reflection and the nonlinearities increase. The normalization procedure did not work well for these highly mismatched contours because of these increased nonlinearities. These nonlinearities seem to be due to third-order intermodulation distortion. The input is matched for the load for maximum power output and then left undisturbed while drawing the contours. So a part of the mismatch is due to the input mismatch. The device should not break into oscillations over any load contours.

Fig. 4(a) shows the constant power contours at 15 percent I_{DSS}. The device is operated under class AB mode. Fig. 4(b) is for the same device with $\sim \frac{1}{2} I_{DSS}$. This is class A mode operation. From the load line and I_{DSS} value, one can calculate a breakdown (gate-to-drain) voltage of more than 15 V. The device has a nominal pinchoff voltage of -2.5 V. Fig. 4(c) is for another device at a class AB bias point (but at a slightly higher percentage of I_{DSS} than in Fig. 4(a)). The bias points chosen for class AB operations happen to yield maximum power added efficiency at 10 GHz. In Fig. 4(b) (the device being operated in class A mode), the contour for 1 dB intersects the axis, $X = 0$, on the Smith chart at points where $|\rho|$ is approximately between 0.40 and 0.45. From (1), these 1 dB points on the $X = 0$ axis have $|\rho|$ equal to 0.45. From [2], $|\rho|$ equals ~ 0.12. It is found that the more the compression level for maximum power, the greater the deviation of the power contours from the small-signal circles, with the power contours falling inside the small-signal circles. In our case, the gain at the maximum power level is 2–3 dB compressed with respect to the small-signal gain. The maximum reactance value for a 1 dB contour, as predicted by [2], is also shown in Fig. 4(b). The maximum reactance values have been projected from the $X = 0$ crossings of the 1 dB contour obtained experimentally. These theoretical limits for maximum $|X_L|$ could not be reached, because the radius of the small-signal 1 dB mismatch circle itself is smaller.

III. Conclusions

An experimental investigation has been made to see if the constant power contours can be normalized at different frequencies at a higher compression point (~ 3 dB). The procedure works fairly well, only under the limitations described in the text. In order to project these contours at frequencies higher than those the load-pull setup is meant for, we must make sure the parasitic and distributed effects are negligible; if they are not, the effective value of C should be calculated at a higher frequency with the parasitic and distributed effects. The value of R can be assumed constant (it has a slight tendency to increase, because of an increase in gate–drain breakdown voltage at higher frequency). The value of maximum power output and the associated gain must be measured separately with a power measurement setup. This can be done with relative ease using small chip tuners inside the carriers. The normalization method described here only draws contours relative to the optimum load for maximum power. Lastly, it should be mentioned that this experimental investigation should not be strictly compared with any analytical way of drawing power contours [4] through the harmonic balance technique [5]. The method works fairly well only if the nonlinearities introduced into the drain current (due to the gate forward conduction, the gate–drain avalanche conduction, and the transconductance) are not large.

Acknowledgment

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